C.2 Concl'd. surface of a corresponding device region.--.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 9-11 and 14-29 are pending in this application. Claims 16-23 have been withdrawn from consideration. Claims 12 and 13 were previously canceled without prejudice or disclaimer. Claims 9 and 25-29 have been amended to even more clearly highlight the present invention without the introduction of any new matter. In addition, since the present amendment to Claims 9 and 25-29 makes the previously claimed range smaller, there can be no new issues raised by these amendments.

In the outstanding Office Action, Claim 14, 15, and 24 were objected to, Claims 9, 11, 14, 15, and 24-29 were rejected under 35 U.S.C. §103(a) as being unpatentable over Bose et al (U.S. Patent No. 5,492,858, hereinafter Bose), and Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Bose in view of the Wolf et al article ("Silicon Processing for the VLSI era", hereinafter Wolf).

Initially, it is noted that FIG. 4 was corrected in the parent application as shown on the sketch accompanying the letter attached hereto requesting examiner approval of the same change to FIG. 4 here. In the parent application, FIG. 4 was noted to be inaccurate relative to the description at page 11, lines 6-10 of the specification that indicates that 50°C intervals are used between 1000°C and 1350°C. In addition, the inaccuracy of the defect density at 1100°C for original FIG. 4 is believed to be clear from the curve itself, as well as from the specification discussion at page 11, lines 30-36 that indicate that the annealing temperature range of the present invention is higher than the annealing temperature range "from 1000 to

1100°C" to acceptably reduce the number of dislocations.

As another initial matter, the objection made as to Claims 14, 15, and 24 is not understood. In this respect, these claims have not been rejected under the second paragraph of 35 U.S.C. §112 which means the PTO does not suggest that these claims need to be modified because those of ordinary skill in the art would find the subject matter of Claims 14, 15, and 24 to be indefinite. It is well established that the statute controls and if the statute has been complied with, PTO requirements cannot be made that demand more than that needed to comply with the statute. See In re Stempel, 113 USPQ 77, 81 ("The patent statutes give to inventors the right to a patent upon compliance with their provisions, and neither the rules promulgated by the Patent Office nor the interpretation placed upon them can detract from these rights.") as well as In re Stephens, 188 USPQ 659, 661 (CCPA 1976) setting forth that a disclosure sufficient to satisfy the statute cannot be the basis for a further requirement by the PTO.

Here, it is clear that Claims 14, 15, and 24 all define "d" and "l" in terms of depth and width of the grooves and that "x" and "y" are used in the standard "x" and "y" coordinate direction sense which is clear from the specification and drawings (Figs. 12A-12C) as well as from common knowledge. The knowledge of the artisan as well as the particulars of the disclosure must always be taken into account. See In re Johnson, 194 USPQ 187, 194 (CCPA 1977).

Before considering the 35 U.S.C. §103 rejections, it is believed that a brief review of the present invention would be helpful. In this respect, Applicants' invention is directed to a method of manufacturing a semiconductor substrate having shallow trench isolation (STI) regions delineating a geometrical pattern of very small feature sizes (such as sub-micrometer

sizes) at a top surface of a device region surrounded by the STI regions forming window portions without generating significant crystalline defects in the device region. The main electrode regions, such as the source/drain regions of an MOS transistor, are selectively formed by diffusing impurity atoms (or by implanting impurity ions) through these window portions.

One important feature of the present inventive method includes the claimed annealing at a temperature T such that $1100°C < T \leq 1300°C$ to insure that the dislocation density generated in the corresponding device region in a vicinity of the grooves of the invention is less than $1/\mu m^2$" in Claim 9 terms. As shown by the curve in Fig. 4, this dislocation density is not achieved at an anneal temperature of 1100°C because the dislocation density at this anneal temperature is $2/\mu m^2$ and the dislocation density does not approach being the required value of less than $1/\mu m^2$ until the anneal temperatures are at least 1150°C, after which the dislocation density gradually decreases. Besides FIG. 4, page 11, lines 30-36 of the specification indicate that the annealing temperature range of the present invention is higher than the annealing temperature range "from 1000 to 1100°C," page 22, lines 15-17 of the specification indicate that "[a]t more than 1100°C from which generation of dislocation is suppressed," and page 12, lines 5-7 of the specification note that the corresponding desired reduced leakage current does not occur unless the annealing is "in excess of 1100°C."

Conventional oxide films have been deposited by organic based CVD and use low temperature processing to achieve small geometric dimensions and a high aspect ratio. The downside discovered by applicants is that poor crystallographic characteristics with stress in these conventional oxide films result in and in turn generate high density crystalline defects in the semiconductor substrate. Thus, while conventional oxide films deposited by organic

silicon based CVD methods including low temperature processing achieve small geometrical dimensions and a high aspect ratio, they do not provide the above noted superior crystallographic structure in terms of the above-noted dislocation density. The conventional films having poor crystallographic structure and higher dislocation densities inherently lead to internal stress which generates large and high density crystalline defects in the semiconductor substrate formed as the device region sandwiched by the grooves. Note, Fig. 2, for example. The stress due to shrinkage caused by dissociation of moisture that is inherently contained in the present day organic silicon source material is what generates many crystalline defects, such as dislocations in the semiconductor substrate.

On the other hand, with the claimed annealing step of the oxide films at the claimed substrate temperature greater than 1100°C but less than or equal to 1350°C, the oxide film is provided containing a "predetermined rate" of higher order ring structures and a "predetermined rate" of lower order ring structures (see Fig. 7A, for example, and note page 22, lines 15-17 stating that "[a]t more than 1100°C from which generation of dislocation is suppressed") and stress in the buried oxide films is relaxed. Therefore, the generation of crystalline defects in the semiconductor substrate is suppressed as shown in Fig. 11, for example, and the dislocation density in a vicinity of the groove becomes less than $1/\mu m^2$ as noted at page 20, lines 33-36 of the specification, for example.,

Further, the annealed oxide film, which is annealed at the claimed substrate temperature of greater than 1100°C but less than or equal to 1350°C, provides an etching rate with ammonium fluoride (NH_4F) solution that is substantially equal to that of the etching rate of a thermal oxide film. Note, for example, Fig. 7B and the description at page 22, line 34 to page 23, line 9 with particular regard to page 23, lines 3-4("substrate temperature over 1100

°C").

Therefore, providing a semiconductor substrate having the claimed geometry of oxide filled isolation grooves around device regions that are annealed at the claimed substrate temperatures provides the advantage of a lower dislocation density and a lower leakage current even with a high packing density being used.

Turning now to Bose et al, there is no disclosure or suggestion of claimed step of annealing at substrate temperatures higher than 1100 °C but lower than or equal to 1350 °C. Since the upper useable annealing temperature suggested by Bose is about 1100 °C, Bose clearly does not teach or suggest any reason to provide annealing at temperatures greater than 1100 °C in terms of achieving the claimed dislocation density (Claims 9, 25, 28, and 29) or higher order and lower order ring structures (Claims 26 and 27).

The contention of the Action that it would have been obvious to determine the optimum annealing temperature for the oxides layer has been noted, but this contention is improper since Bose fail to show any relationship between the annealing temperatures and the dislocation density or order of ring structures in the vicinity of the groove. Note again that Fig. 4 is Applicants' work, as is Fig. 7A. It is well established to be improper to read obviousness into an invention on the basis of an applicant's own statements. Note In re Sponnoble, 160 USPQ 237, 243 (CCPA 1969).

Moreover, while optimization of a known result effective variable has been held to be within the ordinary skill in the art, this doctrine does not apply unless the variable being optimized is one that is recognized in the art as leading to the particular result. See In re Antonie, 195 USPQ 6 (CCPA 1977). Here, the only hint that the use of an annealing temperature in the claimed range provides the benefits of reduced dislocation density and a

lower leakage current even with the high packing density being used is Applicants" disclosure, not that of Bose. The theory that discovery of an optimum or workable range is not inventive does not apply where, as here, there is no knowledge that the annealing temperature being increased above 1100 °C will optimize anything. Accordingly, in view of the fact that the data shown in Figs. 4 and 7A, for example, was not known in terms of increases in annealing temperatures above 1100 °C resulting in improvements in crystallographic structure and measured dislocation density, the optimization theory fails and it is clear that the subject matter of independent Claims 9 and 25-29 is different from and patentable over anything taught or reasonably suggested by Bose.

Thus, while Bosel teaches using a ambient for annealing an oxide film at about of 1100 °C, this alone does not render the subject matter of Claims 9 and 25-29 obvious. As well known in the art, the thermal oxidation rate in such a steam ambient is very high, and having a substrate temperatures higher than 1150 °C is not preferable, since such annealing at higher temperatures in a steam ambient would be expected to generate many crystal defects such as oxidation induced stacking faults (OSFs), in addition to deteriorating the finer geometrical structures deposited by the organic silicon based CVD, with overgrown thermal oxide film. As stated in column 5, lines 41-61, Bose a liner of silicon nitride 18 is used to protect oxidation of the underling silicon and/or thermal oxide, since the thermal oxidation rate in the steam ambient is very high at a temperature of 1100 °C. In this sense, it can be concluded that the optimum annealing temperature for the oxides layer of Bose cannot be in such a higher temperature range exceeding 1100 °C.

In addition, the Action relies upon it being well known in the art to expose the active area after formation of the isolation structure so that active devices can be built thereat. This

contention is incorrect since if the upper parts of the oxide films are removed so as to planarize a surface of a resultant structure until surface areas of the semiconductor substrate are substantially exposed as stated in Claim 9, the exposed surface of silicon substrate 10 is adversely oxidized because the liner of silicon nitride 18 is also removed by the planarizing step. As stated in column 5, lines 41-61, the surface of silicon substrate 10 must always be covered by the liner of silicon nitride 18 during the annealing step so as to avoid Fig. 3 problems. This makes it clear that Bose teaches away from planarizing mesa areas 31, 32, 33, and 34 in the manner suggested in the Action. It defies logic to suggest that all of the Bose reasons for having active mesa areas 31, 32, 33, and 34 would simply be ignored because active devices are to be built, given the well known use of selective etching to form active devices. It is well established that there must be some logical reason apparent from positive, concrete evidence of record which justifies the modification proposed to be obvious, not the exact opposite. See In re Regel, 188 USPQ 136, 139 n.5 (CCPA 1975).

In addition, as stated in Bose at column 5, lines 27-41, the wet etching rate of the nitrogen annealed oxide is *1.4 times* higher than the etching rate for thermal oxide, and Bose generates unwanted seam grooves 15 and edge grooves as shown in Fig. 3. To overcome these flaws, Bose teaches annealing in the steam ambient with the liner of silicon nitride 18, that has no relation with the present invention. That is, only by following the teachings of the present invention does the wet etching rate of the annealed oxide become substantially identical to the etching rate for thermal oxide, another advantage that is not taught or suggested by Bose as logically to be expected as to using annealing temperatures higher than 1100 °C. Moreover, if a temperature about 1100 °C is used, the result will not be the claimed dislocation density as noted above.

Substantially the same arguments made above as to Claim 9 apply also to Claims 11, 14, 15, and 24 which ultimately depend from Claim 9. In addition, these dependent Claims add features, such as to groove structural details in Claims 14, 15, and 24, that are not taught or suggested by Bose. Thus, Claims 11, 14, 15, and 24 are believed to be patentable for the same reasons Claim 9 is as well as because of the features added by each of these claims that further define over Bose.

The proposed combination of Wolf and Bose as to Claim 10 subject matter does not cure the deficiencies noted above as to Bosel since Wolf does not teach or suggest the claimed annealing step being for alleviating crystallographic stress so as to obtain the claimed low dislocation density of less than $1/\mu m.^2$ To whatever extent Wolf teaches a CVD method employing TEOS at table 4, page 194, these teachings do not make those that are missing inconsequential.

Therefore, the rejections applied as to Claims 9, 11, 14, 15, and 24-29 under 35 U.S.C. §103(a) in view of Bose are respectfully traversed and requested to be withdrawn. Similarly, the rejection applied as to Claim 10 under 35 U.S.C. §103(a) in view of the combination of Wolf and Bose is respectfully traversed and also requested to be withdrawn.

Since no other issues are believed to be outstanding in the present application, it is believed to be clearly in condition for formal allowance and an early and favorable action to that effect is therefore respectfully requested.

Respectfully submitted,

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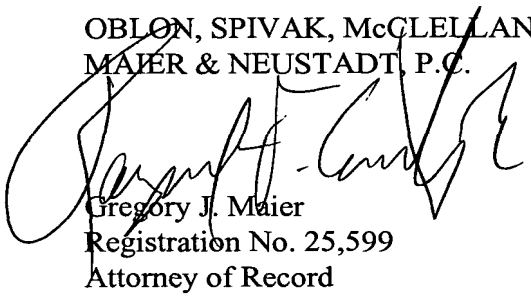

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